

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Akhil K. Garlapati et al.

Assignee: Silicon Laboratories Inc.

Title: VOLTAGE REFERENCE GENERATOR CIRCUIT USING LOW-BETA
EFFECT OF A CMOS BIPOLAR TRANSISTOR

Patent No.: 7,321,225 B2 Issued: January 22, 2008

Atty. Docket No.: 026-0044

January 24, 2008

ATTN: Certificate of Correction Branch
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT –
PTO MISTAKE (37 C.F.R. § 1.322(a))**

Dear Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322(a), please issue a Certificate of Correction in the above-identified matter. The mistake(s) to be corrected was made by the Office.

1. Attached hereto is Form PTO/SB/44 (PTO-1050) suitable for printing.
2. The exact page(s) and line number(s) where the error(s) is shown correctly in the application file:
Response filed August 2, 2007, page 5, line 12 of Claim 26
3. Please send the Certificate to:

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Respectfully submitted,



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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO: 7,321,225 B2
APPLICATION NO.: 10/813,837
ISSUE DATE: January 22, 2008
INVENTOR(S): Akhil K. Garlapati et al.

It is certified that error(s) appear(s) in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 8, line 32, please replace "minored" with --mirrored--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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